

# **A METHOD FOR FORMING CAPACITOR OF SEMICONDUCTOR DEVICE**

## **BACKGROUND OF THE INVENTION**

### **1. Field of the Invention**

5           The present invention generally relates to a method for forming a capacitor of a semiconductor device, and more specifically, to a method for forming of a capacitor wherein an etching barrier layer comprising a stacked structure of a nitride film and a tantalum oxide film is  
10 employed to prevent cracking and to provide sufficient support for storage electrode.

### **2. Description of the Prior Art**

          As the size of a cell decreases due to a high  
15 integration density of a semiconductor device, it becomes more difficult to obtain sufficient capacitance which is proportional to a surface area of a storage node.

          In particular, in the DRAM wherein a unit cell includes a MOS transistor and a capacitor, a capacitance of  
20 the capacitor needs to be increased and an area occupied by the capacitor needs to be decreased to achieve high integration.

          In order to increase capacitance  $C$  of a capacitor which follows the equation of  $(\epsilon_0 \times \epsilon_r \times A)/T$  ( $\epsilon_0$ : vacuum

dielectric constant,  $\epsilon_r$ : dielectric constant of dielectric film, A: area of storage electrode, T: thickness of dielectric film), there are proposed methods of using a dielectric film having a high dielectric constant, of  
5 reducing the thickness of the dielectric film, or of increasing a surface area of a storage electrode.

A conventional method for forming a concave-type (or cylinder-type) capacitor (not shown) is as follows.

A device isolation film, an impurity junction region,  
10 a word line, a bit line and a contact plug for storage electrode are formed on a semiconductor substrate. Then, an interlayer insulating film is formed on the resulting structure.

A nitride film having a thickness of less than 1000Å,  
15 which is an etching barrier layer, is formed on the resulting structure.

An oxide film for storage electrode is formed on the nitride film. The oxide film has a thickness of more than 15000Å and consists of BPSG, PSG or TEOS.

20 Thereafter, the oxide film for storage electrode is etched via a photolithography process using a storage electrode mask to form a storage electrode region exposing the storage electrode contact plug.

A conductive layer for storage electrode connected to

the storage electrode contact plug is formed on the entire surface of resulting structure including the storage electrode region.

Next, a photoresist film filling the storage  
5 electrode region is formed on the entire surface of the resulting structure, and then planarized to expose the oxide film for storage electrode.

Thereafter, the photoresist film is removed so that only a portion of the conductive layer for storage  
10 electrode on the surface of the storage electrode region remains. The oxide film for storage electrode is then removed to form a concave-type storage electrode. The process of removing the oxide film for storage electrode is performed using BOE solution. The nitride film, which  
15 serves as an etching barrier layer, is damaged during the process.

A dielectric film is formed on the surface of the storage electrode, and an annealing process then is performed. The annealing process is performed under an  
20 oxygen atmosphere at a temperature higher than 700°C. During the annealing process, cracks are generated in the damaged nitride film, and thus the nitride film cannot support the storage electrode. As a result, the storage electrode collapses, which leads to bridging between

adjacent storage electrodes. Moreover, oxygen atoms penetrate through the cracks to oxidize a lower bit line.

A plate electrode is then formed to complete the formation of a capacitor.

5        Fig. 1a is a photograph showing a cross-section of a conventional capacitor of a semiconductor device wherein the lower bit line is oxidized by the oxygen atoms.

Fig. 1b is a plane view illustrating the structure of the conventional capacitor shown in Fig. 1a.

10       Fig. 2 is a photograph showing a plane view of the conventional capacitor of a semiconductor device wherein bridging between adjacent storage electrodes due to lack of support by the etching barrier layer are shown.

As described above, according to the conventional  
15    method for forming a capacitor device, the nitride film serving as an etching barrier layer is damaged in the process of removing the oxide film for storage electrode. This damage causes bridging between adjacent storage electrodes. Moreover, cracks in the etching barrier layer  
20    generated during the annealing process causes oxidation of lower conductive layers due to oxygen atoms penetrating through the crack.

As a result, characteristics and reliability of semiconductor device are degraded, and high integration of

the semiconductor device cannot be achieved.

#### **SUMMARY OF THE INVENTION**

It is object of the present invention to provide a  
5 method for forming a capacitor of a semiconductor device  
wherein an etching barrier layer having a stacked structure  
of a nitride film and a tantalum oxide film is formed to  
prevent penetration of oxygen, thereby inhibiting oxidation  
of an electrode, and to relieve the stress of the nitride  
10 film, thereby preventing a crack.

The method for forming a capacitor of a semiconductor  
device, comprising the steps of: forming an etching barrier  
layer on an interlayer insulating film having a storage  
electrode contact plug therein, the etching barrier layer  
15 comprising a stacked structure of a nitride film and a  
tantalum oxide film; forming an oxide film on the etching  
barrier layer; selectively etching the oxide film and the  
etching barrier layer to form an opening exposing the  
storage electrode contact plug; depositing a storage  
20 electrode layer on the bottom and the inner walls of the  
opening; and removing the oxide film, whereby forming a  
storage electrode is provided.

#### **BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1a is a photograph showing a cross-section of a conventional capacitor of a semiconductor device.

Fig. 1b is a plane view illustrating the structure of the conventional capacitor shown in Fig. 1a.

Fig. 2 is a photograph showing a plane view of the conventional capacitor of a semiconductor device.

Figs. 3a through 3c are cross-sectional diagrams illustrating a method for forming a capacitor of a semiconductor device according to a preferred embodiment of the present invention.

Fig. 4 is a graph showing the stress of a tantalum oxide film according to the temperature in a thermal treatment process.

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#### **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS**

The present invention will be described in detail with reference to the accompanying drawings.

Figs. 3a through 3c are cross-sectional diagrams illustrating a method for forming a capacitor of a semiconductor device according to a preferred embodiment of the present invention.

Referring to Fig. 3a, a device isolation film (not shown), an impurity junction region (not shown), a word

line (not shown) and a bit line (not shown) is formed on a semiconductor substrate 11. An interlayer insulating film 14 including a contact plug 13 for storage electrode is then formed on the semiconductor substrate 11. Thereafter,  
5 an etching barrier layer consisting of a stacked structure of a nitride film 15 and a tantalum oxide film 17 is formed on the entire surface of the resulting structure.

The nitride film 15 is preferably formed via a LPCVD or a PECVD method. The LPCVD process is performed in a  
10 furnace at a temperature ranging from 600 to 800°C using DCS and  $\text{NH}_3$  or in a single chamber at a temperature ranging from 550 to 800°C using  $\text{NH}_3$  and a gas selected from the group consisting of  $\text{SiH}_4$ ,  $\text{Si}_2\text{H}_6$  and combinations thereof. The PECVD process is performed by exciting plasma at a  
15 temperature of lower than 600°C under an atmosphere of a mixture gas of a gas selected from the group consisting of  $\text{SiH}_4$ ,  $\text{Si}_2\text{H}_6$  and combinations thereof, and a gas selected from the group consisting of  $\text{NH}_3$ ,  $\text{N}_2$  and combinations thereof.

20 The tantalum oxide film 17 is preferably in amorphous state and the detail of the formation process thereof is as follows.

A chemical such as  $\text{Ta}(\text{OC}_2\text{H}_5)_5$  is supplied to an evaporator via a flow rate controller such as an LMFC

(liquid mass flow controller) and then evaporated at a temperature ranging from 120 to 200°C to form a chemical vapor containing Ta. Since the evaporation temperature of  $\text{Ta}(\text{OC}_2\text{H}_5)_5$  is higher than 110°C, the evaporation process  
5 should be performed at a temperature higher than 110°C.

Thereafter, the chemical vapor containing Ta and excessive oxygen gas which is a reaction gas is supplied to a LPCVD chamber at a flow rate ranging from 10 to 1000sccm and at a temperature ranging from 300 to 600°C to induce  
10 surface reaction, thereby forming the tantalum oxide film 17 in amorphous state.

In one embodiment, the tantalum oxide film 17 may be formed using only  $\text{Ta}(\text{OC}_2\text{H}_5)_5$  source, or TaON may be used instead of the tantalum oxide film using a Ta source and a  
15  $\text{NH}_3$  source gas as reaction gases.

In another embodiment, the nitride film 15 and the tantalum oxide film 17 may be formed in one system such as (a) or (b).

(a) a tantalum oxide film deposition chamber and a  
20 nitride film deposition chamber are configured to constitute a multi-chamber in one system. PECVD or LPCVD methods are preferred.

(b) The nitride film 15 and the tantalum oxide film 17 are formed in the same chamber. In this case, the



nitride film 15 is first deposited via a PECVD process using a gas selected from the group consisting of  $\text{SiH}_4$ ,  $\text{Si}_2\text{H}_6$  and combinations thereof in a tantalum oxide film deposition chamber and adding an  $\text{NH}_3$  line thereto, and then  
5 the tantalum oxide film 17 is deposited after a purge process.

Since the tantalum oxide film deposition chamber is maintained at a low temperature, and a plasma can be excited therein, a film is not deposited easily via a LPCVD  
10 process. However, since only PECVD process is used to form the nitride film 15, the nitride film 15 and the tantalum oxide film 17 can be formed in the tantalum oxide film deposition chamber having a low temperature.

Referring to Figs. 3b and 3c, an oxide film 19 for  
15 storage electrode is formed on the tantalum oxide film 17. Preferably, the oxide film 19 has a thickness of more than  $15000\text{\AA}$ , and consists of oxide films containing impurities such as BPSG, PSG or TEOS.

Thereafter, the oxide film 19 is selectively etched  
20 via a photolithography process using a storage electrode mask to form an opening 21 exposing the storage electrode contact plug 13. A conductive layer (not shown) for storage electrode is formed on the entire surface of the resulting structure including the surface of the opening 21. A

photoresist film (not shown) filling the opening 21 is then formed on the entire surface of the resulting structure.

Next, the entire surface is planarized to expose the oxide film 19 for storage electrode. Thereafter, the photoresist film and the oxide film 19 for storage electrode are removed to form a concave-type storage electrode 23. The process of removing the oxide film 19 for storage electrode is preferably a etching process using BOE solution.

Thereafter, a dielectric film (not shown) is formed on the surface of the storage electrode 23, and then subjected to an annealing process. The annealing process is preferably performed under an oxygen atmosphere at a temperature higher than 700°C. A plate electrode(not shown) is formed on the dielectric film to complete the formation of a capacitor.

Fig. 4 is a graph showing the stress of a tantalum oxide film according to the temperature of an annealing process. It should be noted that the stress decreases as the temperature is increased.

As discussed earlier, according to the method for forming a capacitor of a semiconductor device of the present invention, an etching barrier layer having a stacked structure of a nitride film and a tantalum is

formed to prevent damage of the nitride film and collapse of a storage electrode, thereby providing a capacitor having sufficient capacitance for high integration of a semiconductor device.

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